

Asynchronous Circuits as an Enabler of Scalable and Programmable Metasurfaces

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Abstract—Metamaterials and metasurfaces have given possibilities for manipulating electromagnetic (EM) waves that in the past would have seemed impossible. The majority of metasurface designs are suitable for a particular frequency and angle of incidence. One long-sought objective is the design of programmable metasurfaces to dynamically manipulate a variety of incoming EM frequencies and angles. In order to do this, a large-scale mesh of networked chips are required below the metasurface, which apart from adapting electrical impedance properties, also communicate with each other, thus relaying information about meta-atom settings, as well as forwarding possible distributed measurements taken. This paper describes why an asynchronous mixed-signal ASIC is advantageous for the control of scalable, EM absorbing, metasurfaces.

I. INTRODUCTION

METAMATERIALS are artificial structures engineered to exhibit EM properties not commonly found in nature. Permittivity (ϵ) and permeability (μ) in naturally occurring materials such as glass or water are mostly positive. However, some metals such as silver and gold have negative permittivity at short wavelengths whilst materials such as a surface plasmon have either ϵ or μ negative. What is important though is that there are no materials having both ϵ and μ negative. Such metamaterial structures, can be fabricated, to have negative ϵ and negative μ , something that Veselago[1] predicted back in 1968. In 2001, Smith et al. [2] with the first experiments in microwaves, showed a pass band in various samples, where both ϵ and μ appeared to be negative, thus also giving a negative refractive index. Since then, these structures have shown extraordinary EM properties, and numerous novel devices have been reported in the literature e.g. invisibility cloaks [3], leaky-wave antennas [4], super-lenses [5], anomalous reflectors [6][7] and perfect absorbers [8], all demonstrating unnatural functionalities. Most of these metamaterial/metasurface structures have a fixed function configured for a very narrow frequency and angle of incidence, with no means of reconfiguring properties once fabricated.

One attempt to make these materials reconfigurable used mechanical elements, which when placed under stress, change shape [9], however this approach has very limited reconfigurability. More recently electrically reconfigurable, programmable [10] [11] metamaterials have emerged, where a digital signal is used to change the voltage bias of a diode-based capacitor, hence giving two different capacitive states to the metamaterial atom (meta-atom). Although a major step forward, this solution still has major limitations in tuneability, given only two possible states for the meta-atom.

This paper advocates the use of asynchronous digital circuits in the development of an application specific integrated circuit (ASIC), to be embedded within metasurface structures,

in order to give multiple degrees of freedom in the adaptability of the meta-atoms. These ASICs must also include mini-routers to move information through an arbitrarily-large meta-atom array, so as to be able to configure the complex load impedances at the different locations of the metasurface. Section II describes the system structure and constraint requirements in which the ASICs need to operate within, whilst Section III describes how the asynchronous communication scheme is better suited to address these challenges and why it is preferred over its synchronous counterpart.

II. SYSTEM STRUCTURE

A. Overview

The system structure of a programmable metasurface, as shown in Figure 1, requires at least a 3 layer PCB, where the top-layer consists of an array of metal patches, e.g. as in [12], the intermediate layer consists of a ground plane and the bottom layer consists of an array of ASICs, connected through vias to the top metal patch layer. The top layer is patterned according to the EM function to be implemented; options include anomalous reflection or absorbance. The intermediate layer is a ground plane so as to minimise the effect of the surface that metasurface conforms to. Finally, the ASICs role is to adapt the EM properties of the top-layer by providing adjustable complex-impedance loading, as well as networking functionality. The networking is required in order to receive and relay incoming commands. To keep the metasurface ASICs as simple as possible, a shared gateway connects the driving computer to the array. Figure 1 shows a possible configuration where an array of 3×3 ASICs (on the bottom layer) form a tile that consists of 6×6 metal patches on the top layer. After computing the metasurface configuration, based on incoming frequencies and angle of incidence information, the computer sends configuration settings, as desired complex impedance information for each meta-atom, to the tile via a wireless gateway. This gateway also supplies power to the metasurface ASICs via wired connections on the bottom plane. The tiles are such that an arbitrary number tiles can be clipped together to increase the size and shape of the overall metasurface.

B. Requirements/Constraints

The first metasurface prototype targeted by this work involves an adaptive absorber/anomalous reflector, for various angles of incidence. Its use might be for reducing interference of wifi signals, reducing human exposure to stray wifi signals over health concerns or even to intelligently reflect a wifi signal in a particular direction, so as to boost reception. In order to achieve this functionality, one needs adaptability for both active (resistive) and reactive (capacitive/inductive) components linking adjacent patches. To program the active

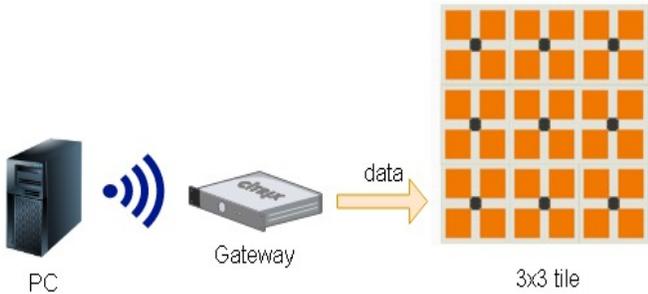


Fig. 1: Top Level System Architecture. After computing the metasurface configuration the computer sends the instructions wirelessly to the gateway that is physically located on the edge of the metasurface, which in turn sends instructions to the ASICs to configure their local meta-atom.

and reactive components, a mixed-signal ASIC containing digitally controlled varactors and varistors is required. Furthermore, this ASIC must be able to communicate digitally with its adjacent neighbours in order to be able to pass on commands that are not destined for itself or in order to send messages to the gateway that concern a local measurement or event, such as a failure. Thus, key architectural choices must be made for these ASICs, taking into account the various requirements/constraints listed below:

- **Meta-atom Size**

Today wifi signals' frequency range varies between 2.4GHz (IEEE 802.11b) and 60GHz (IEEE 802.11ad), thus ranging in wavelength from 12.5cm to 5mm respectively. In general, there should be *at least* 5 meta-atoms per wavelength for correct operation and the tile length should include *at least* 5×5 wavelengths for reasonable two-dimensional directivity. Thus scaling up the frequency of operation tightens the size constraints for the ASICs, given that the wavelength becomes smaller and the meta-atom needs to decrease in size; this is below $1\text{mm} \times 1\text{mm}$ in the IEEE 802.11ad case. In this limited footprint, the meta-atom needs to accommodate the metal patches, all necessary components to tune the complex impedances between the patches, the control and communication circuitry, the pins and tracks to neighbouring meta-atoms and any other "packaging inefficiencies". This makes the use of multiple components per meta-atom extremely challenging and thus directs towards a single chip ASIC for each meta-atom on the PCB.

- **Conformal Metasurface**

In order to enable the metasurface to be applied to surfaces other than walls, e.g. on a vehicle, it is desired that the adaptive meta-atoms are designed on a flexible or rigid-flex PCB substrate.

- **Scalability**

The tile must be easily scalable. By adding or removing metasurface patches, it should automatically be adjusted to recognize the number of patches in the tile and scale the addressing accordingly.

- **Low Cost**

The cost of a tile, and consequently the whole metasurface, must be low enough to be adopted. There is no point in engineering adaptive metasurfaces that can not be used due to prohibitive costs. This translates to as few components as necessary and to using a semiconductor technology that is not exotic and thus expensive. Furthermore the cost can be reduced if a single design of meta-atom ASIC, can cater for all cases in the array e.g. not have a different ASIC for the edges of the metasurface structure or for interfacing to the gateway.

- **Power consumption**

The need for low power consumption is a fundamental limitation for most of the integrated circuits, but this is especially pertinent given the large surfaces to be covered and where the power can scale up very quickly. The power needs to be supplied by the gateway or if possible through energy scavenging techniques.

- **EM emissions**

The circuitry that enables the adaptability of the absorber/anomalous reflector should have minimal or if possible zero EM emissions so as to avoid interfering with the incident wave through reflections off the covered surface. A large surface that is clocked could end up radiating a large amount of energy into an area that was supposed to eliminate existing EM signals, and hence exasperate the problem that was to be solved.

- **Timing Constraints**

In a synchronous ASIC digital solution, part of the design methodology requires the synthesis of a clock tree that is scalable. It should also satisfy the requirements of a flexible metasurface where tiles are connected together to create a surface as large as a wall and possibly conforming to irregular shapes. The clock tree should be resilient to process variability as well as variability in the overall metasurface. Thus it should provide margins for both intra and inter die communications. Furthermore, the clock skew needs to be well controlled in order to prevent the violation of the setup and hold time constraints. Given that the same dies should be "generic" in the sense that they may be used to populate different metasurface designs this is not trivial, if not impossible. Today's design tools are optimised for synthesizing clock trees on a single chip and at most to the area of a motherboard. Furthermore, it has been reported [13] that in modern chips, in order to conform to timing constraints, an elaborate clock tree is synthesised such that as much as 40% of the total power consumption is utilized by just the clock-tree. An alternate solution would be to use a crystal oscillator in each meta-atom, and use a phase-locked loop to bring all clocks in sync. However, since crystals are relatively expensive and their sizes are at least a few mm in size this is not a viable solution.

The above constraints make an asynchronous-digital based, mixed-signal ASIC an attractive solution. Though an approach that is not used often, due to the design complexity and

the lack of the commercially available tools for automated synthesis, for this application asynchronous design seems to be the most suitable choice. The next section describes the characteristics of asynchronous circuits and why they are an enabling technology for this application.

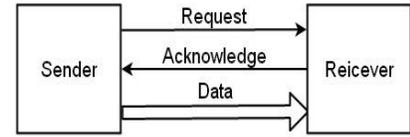
III. ASYNCHRONOUS VS SYNCHRONOUS FOR ADAPTIVE METASURFACE ASICS

The meta-atoms' ASICs require a mixed-signal solution where a number of D/A converters are used to control varactors and varistors inserted in the RF signal paths. The choice of the type of digital design is a key aspect that defines the viability of a highly adaptive metasurface. Digital circuit design can be divided into two opposing methodologies, that concern timing constraints. The most dominant approach is that of synchronous circuits, whereby signals synchronise changes of states across the entire chip, at discrete points in time. The global clock is therefore a really powerful technique for simplifying the implementation of sequencing circuits. However, as the size of a system increases, the common and discrete notion of time becomes more difficult to achieve, especially when the size of the system can vary dynamically. Asynchronous circuits are different. There is no common and discrete time. For the communication between components, handshaking is used to coordinate the movement of information and computation. In the following section a brief introduction to the basic asynchronous circuits is presented and the suitability, as opposed to a synchronous design, for large adaptive metasurfaces is discussed.

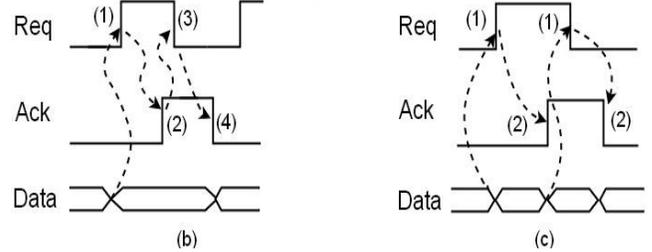
A. Introduction to Asynchronous Circuits and Handshaking

The principle behind asynchronous logic design is that each block or subsystem only communicates with adjacent blocks when the exchange of information information is desired. The communication does not have to wait to be triggered at every clock cycle but can occur at arbitrary times. The key element making this possible is the *handshake*.

A variety of handshake protocols have been reported in the literature [14]. The most common being the four-phase and the two-phase bundled data protocols. Both protocols utilize the request and acknowledge signals, along with a data line or a data bus as shown in Figure 2a. The four-phase communication protocol, illustrated in Figure 2b goes as follows: (1) once the data is made available on the data line, the sender (left) sets the request HIGH and (2) when ready, the receiver latches the data and sets the acknowledge HIGH, (3) the sender then takes request LOW and (4) the receiver retracts the acknowledge signal going back LOW, opening the way for a new communication to begin. The four-phase bundled data protocol has the advantage that the handshake circuits are very simple, but has the disadvantage of using unnecessary time and power for lowering the two signals. This could be avoided by using the two-phase bundled data protocol (Figure 2c) since with this protocol, it is each signalling transition 0→1 and 1→0 that represents the event, rather than the actual level on the request and acknowledge lines. Two-phase signalling requires slightly more complex circuits to be implemented. There are other protocols, e.g. single rail encoding, dual rail encoding, etc, with other pros and cons, however these will not be elaborated here.



(a)



(b)

(c)

Fig. 2: (a) The communication scheme between the sender and the receiver using the request and acknowledge signals, (b) the four-phase protocol signal transition for one event and (c) the two-phase protocol signal transition for one event.

At the circuit level, an important building block is the Muller-C element, which in its basic form changes its output only when all the inputs “agree” i.e. if all inputs are zero then the output transitions to zero, if all inputs are 1 then the output transitions to 1, for anything else, the state of the element remains the same. It is very useful for creating a signal to indicate when all parallel threads have been completed, in addition to implementing more simple handshakes.

Figure 3 shows the implementation of the handshake circuit between two modules. The function blocks start their operation once the request signal has been received. The delay block is added to prevent enabling (request signal high) the latch before the data are ready to be stored. Then the Muller-C element is enabled and the data are stored and move to the next block (if needed). Once the Muller-C element goes HIGH, the acknowledge signal is sent back to the previous controller to inform that the data have been received.

A variety of asynchronous circuits have been presented over the years exploiting the circuit level handshake communications and enabling data driven asynchronous circuit design. Fast and low power microprocessors [15], 3D image processors [16], filter banks for digital hearing aid [17] and wireless endoscopic capsule [18] are some of the applications. Their characteristics are known but they have not been adopted for mainstream applications.

B. The Case for Asynchronous ASICs in Metasurfaces

Although synchronous digital is by far the most predominant methodology used today, there are special cases where the inconvenience of not having commercial CAD tools and readily available libraries to automate the design process, is still not an issue. In the case of an adaptive metasurface ASIC, the difficulty of producing a reliable clock signal over such a large surface makes the asynchronous route look attractive since asynchronous signalling [15] can easily cope with added parasitics or extended/flexed external communication lines

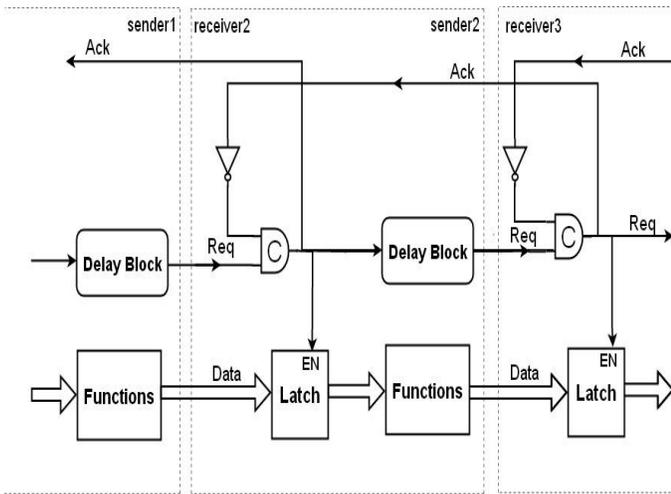


Fig. 3: The four-phase bundle-data implementation. The request signal is being delayed until the function block is finished so as to keep synchronization between the data and the handshake signals.

needed on a conformal metasurface, as long as these affect the data and handshaking lines equally. This property stems from the circuits inherent delay-insensitivity [19][20]. In such a case the handshake process may be slowed down, however it will conclude successfully. This argument also applies to easy scalability, since *composing asynchronous systems is simply a matter of connecting the proper modules with matching interfacing specifications* [21]. This leads to ease of incremental improvement, better technology migration and be able to reuse most of the modules. Furthermore, an asynchronous solution means that there is *no reason to include crystal based oscillators* within the dense array, thus saving space and reducing the cost. Typically a crystal oscillator measures a few mm^2 in size that is comparable to size of the ASIC.

Asynchronous circuits are considered to be *extremely energy-efficient* since they only charge and discharge capacitive nodes when they have to. Systems driven by a clock consume power every time there is a clock event even if no data has changed thus wasting energy. It is possible to have multiple clock domains and to disable parts of the clock tree, however such methods need elaborate control schemes to be driven at a high level. As an example of low-power application, Paver [22] presented an asynchronous version of a microprocessor, which is one of the most energy-efficient microprocessors compared to both synchronous and asynchronous schemes. If an older or low-power semiconductor technology with higher thresholds is chosen then device leakage can be considered negligible and so when no settings in the metasurface are being changed the power consumption is negligible.

A recent work in the University of Utah [23] compares the same microprocessor first by using a clocked network and then by using a control path. The results show a 5% smaller area for the asynchronous design (control path) but with a slightly higher leakage energy due to more buffers that have been used. What is more important though is the 10 times average reduction in power. At a time where the power dissipation is the most significant limitation in circuits, being able to achieve

10 times less power dissipation is a huge step forward in the digital world.

Electromagnetic emissions in asynchronous circuits have been shown to be less than the synchronous counterparts [24] whilst also giving more *evenly spread emissions* [25]. This is expected since by not synchronising all switching activity the signals can not all add up by being in phase. Asynchronous circuits are considered *faster* [26] compared to the synchronous because they exhibit *average-case behaviour* instead of being driven by a clock that assumes worst-case behaviour for all blocks. They also have completion detection mechanisms to detect when an operation is finished, which means the next operation can start. Digital asynchronous circuits have the added advantage of generating less power supply noise [20], when compared to their synchronous counterpart given that the current draw is better distributed in time.

IV. CONCLUSION

In this paper, we have presented a targeted architecture of a large, adaptive metasurface that can both absorb or anomalously reflect EM waves, that has particularly challenging requirements and physical constraints that make designing with a synchronous methodology very difficult. As a result, we introduced and explored the properties of asynchronous digital circuits as an enabling technology for programmable metamaterials, with clear benefits with regards to doing away with the global clock to achieve delay insensitivity, low EM emissions and low power, amongst other benefits.

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